INTERBUS

Conformance Test

Basic Test

Manufacturer Declarations

The "test steps" for the test object are described in the second column and the number of the relevant checklist is given in the first column. The person carrying out the test only has to enter the test result in the "OK" column. Any comments are entered in the "OK*)" field. The assigned text appears at the bottom of the table as a footnote.

No.	Test Step	OK *)

The following applies to the assessment of the test steps:

Y Yes: Criterion met.
All specifications for this test step must be met.

Y- Yes-: Criterion met - deviation permitted.
For deviations that influence neither the electrical nor the time response of the interface, the person carrying out the test may positively assess this part of the test.
Example: Pull-down resistor of 2.7 kOhm instead of 3.3 kOhm is used.

N No: Criterion not met, deviation not permitted.
According to the person carrying out the test, the deviations influence the electrical or time response of the interface in such a way that the test step must be assessed negatively.

/ Inconclusive: Criterion not to be taken into consideration.
The criterion does not apply to the test object and this test step is not relevant to the overall assessment.

For the overall assessment criterion to be "Passed", each test step must receive either the "Criterion met" or "Criterion met - deviation permitted" assessment. If deviations are detected, they must be noted and the final decision must be justified.

Manufacturer Declaration for Devices With RS-485 Copper Interface and Basic Test

Test report number:

No.	Test Step	OK *)
HE 1.	**RS-485 driver/receiver** - **Has an** approved type or alternative *) been used with the specified circuit for the RS-485 driver/receiver in the INTERBUS data path? - Which? (please enter here)	
HE 2.	All resistors have a tolerance of +/-1%.	
HE 3.	**Optocoupler** - **Has an approved type** or alternative *) been used with the specified circuit for the optocoupler in the INTERBUS data path? - Which? (please enter here)	
HE 4.	- Does the series resistor in the LED circuit correspond to the value specified for the optocoupler?	
HE 5.	- Does the pull-up resistor at the output of the optocoupler correspond to the value specified for the optocoupler?	
HE 6.	- Is each optocoupler equipped with a 100 nF blocking capacitor?	
HE 7.	Connector pin assignment - Has an approved type of connector with defined pinning (labeling, assignment, order of the connections especially for the terminals) been used? *) - Which? (please enter here)	
HE 8.	**Additional wiring for** INTERBUS data lines - Have any other active or passive components (e.g., Transsorb or suppressor diodes, filters, etc.) been used on/in the INTERBUS data path in addition to those listed?	

HE 9.	**24 V supply voltage loop** from input to output - All 3 signals FE, +24 V, and 0 V must be looped through without any additional elements (fuses, resistors, etc.) from the input to the output.	
HE 10.	- The 24 V supply voltage connection must be designed according to the defined continuous current. - Installation remote bus I_{Nom} = 4.5 A	
HE 12.	- The 24 V supply voltage connection must be designed according to the defined continuous current. - Rugged Line I_{Nom} = 16 A	
HE 13.	**Data connection from the Rugged Line connector** - The length of the shielded cable from the Rugged Line connector to the device electronics should not exceed 20 cm (7.87 in.).	
HE 14.	HE 1.	
HE 15.	- The isolation voltage between the individual electrically isolated areas is at least 350 V AC.	
HE 16.	- *) If FE of the outgoing interface is not directly connected with GND, a capacitor/resistor combination (R <= 1 MOhm, C approximately 15nF) (parallel circuit) can be selected as an alternative. **HE** 2.	
HE 17.	- Has an approved type of protocol chip or an approved alternative been used? *)	
HE 18.	- If the chip has optical control, is it disabled? (RF1=RF2=1 for SUPI3 OPC)	
HE 19.	- Are all the unused inputs for the protocol chip (including MFPs) connected with a defined voltage?	
HE 20.	**- 3Chex -** **For remote bus** devices (for devices with special requirements, only is approved by the INTERBUS Club.)	
HE 21.	- During bus startup, the Generation 4 master reads in the "Microprocessor Not Ready" ID code and generates the "Incorrect initialization of the protocol chip by the microprocessor" error message 0C73 and 0D70 ..0D73	

HE 22.	- The expected ID code can be read in after bus startup.	
HE 23.	- The power-up reset input of the slave protocol chip and the assigned expansion blocks are wired with a 1 kOhm, 100 nF filter.	
HE 24.	- The voltage monitoring circuit ensures that the reset input for the protocol chip and the assigned expansion blocks has a low signal with a voltage of U Nom minus the tolerance (5 V - 10%, typical).	
HE 25.	- The reset time realized by the voltage monitoring circuit is at least 2 oscillator clock cycles (125 ns at 16 MHz, typical) for the balanced oscillator and at specified voltage.	
HE 26.	- For direct and indirect wiring of the reset input, ensure that the components used in the entire voltage area of the voltage monitor are operating properly. Standard logic gates are **not** suitable.	
HE 27.	- The power-up reset of the slave protocol chip and the assigned expansion blocks is never influenced by the software, an LCA or microprocessor.	
HE 28.	- The resistance between +5 V and the reset pin of the IBS SUPI 3 OPC protocol chip family is **never** lower than 600 Ohm.	
HE 29.	- When using the reset pin of the IBS SUPI 3 OPC protocol chip family as an input: The resistance between GND and the reset pin of the protocol chip does not exceed 600 Ohm on a "0" signal.	
HE 30.	- When using the reset pin of the IBS SUPI 3 OPC protocol chip family as an output: The resistance between GND and the reset pin of the protocol chip is not less than 23 kOhm.	
HE 31.	- A clock (e.g., quartz oscillator) applied at the protocol chip meets the requirements given in the INTERBUS protocol chip data sheet. **)	
HE 32.	- A quartz used meets the requirements given in the INTERBUS protocol chip data sheet. ***)	

HE 33.	- A quartz oscillating circuit does not supply other components with its clock.	
HE 34.	- The clockline is not influenced by other logic or software.	
HE 35.	- The clockline circuit is tested for the entire permissible temperature range of the device +/- 10%.	
HE 36.	- Additional capacitors for the IBS SUP13 quartz OPC quartz inputs are not available.	
HE 37.	- Have approved types or an approved alternative been used for the expansion blocks? *)	
HE 38.	- One data output for the register expansion does not drive more than 4 inputs.	
HE 39.	- If a buffer is used for the register expansion signal ClkExR, have identical buffers been used for signal ToExR2?	
HE 40.	- Are the register expansion registers in close proximity to the protocol chip on the same board? The tracks are < 5 cm (1.97 in.).	
HE 41.	- Are the Latch, Data (IN&OUT), Clock, and /ResReg signals for the register expansion blocks only used by the INTERBUS slave protocol chip or by the reset logic that controls it?	
HE 42.	**Diagnostic signals** - The required diagnostic LEDs for this device type (see table) are directly connected to the slave protocol chip and are not controlled via software (with the exception of TR). *)	
HE 43.	- The green U_L LED is directly controlled by the voltage monitor.	
HE 44.	- If the protocol chip diagnostic input *I/O Error* ("/StatErr" for IBS SUPI 3) is used, the events that are generated by these diagnostic messages are simulated and the response is checked at the INTERBUS master. ****) The data pattern 0xF0 is output for all OUT data bytes of the test object. This means it is also possible to test module error messages by short-circuiting a digital output.	

HE 45.	- If the protocol chip diagnostic input *Reconfiguration Request* ("Conf" for IBS SUPI 3) is used, the events that are generated by this diagnostic message are simulated and the response is checked at the INTERBUS master. ****)	
HE 46.	- If the protocol chip diagnostic input *MAU Warning* ("MAUWS, MAUWR, MAUWH" for IBS SUPI 3) is used, the events that are generated by this diagnostic message are simulated and the response is checked at the INTERBUS master. ****)	
HE 47.	- If the protocol chip diagnostic input *Microprocessor Watchdog* ("/StatErr" for IBS SUPI 3) is used, the events that are generated by this diagnostic message are simulated and the response is checked at the INTERBUS master. ****)	
HE 48.	- If the protocol chip diagnostic output *Alarm* ("Alarm" for IBS SUPI 3) is used, the events that are generated by this diagnostic signal at the device are checked. ****)	
HE 49.	- If the protocol chip diagnostic output *Module Acknowledge* ("/ModAck" for IBS SUPI 3) is used, the events that are generated by this diagnostic signal at the device are checked. ****)	
HE 50.	Additional PCP error **codes** - Additional PCP error codes defined by the manufacturer are always assigned error class "8", error code "0" in the additional code.	

Test object (only for PCP devices)

Manufacturer

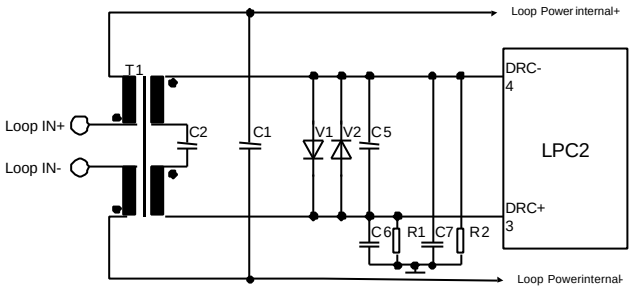
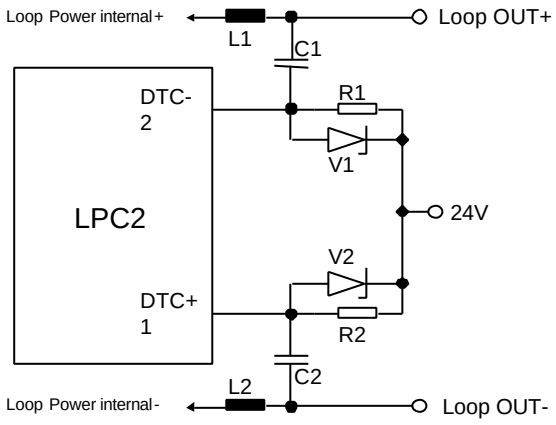
Name

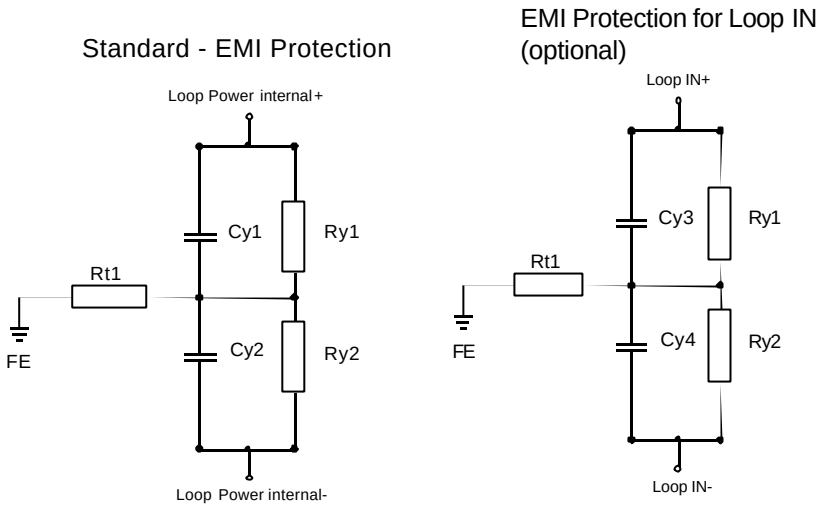
Signature

Manufacturer Declaration for Devices With INTERBUS Loop Interface

Test report number:

No.	Test Step	OK *)
HE 1.	- The isolation voltage between the individual electrically isolated areas is at least 350 V AC.	
HE 2.	- Are all the unused inputs for the protocol chip (including MFPs) connected with a defined voltage?	
HE 3.	- 3Chex - For remote bus devices (for devices with special requirements, only is approved by the INTERBUS Club.)	
HE 4.	- During bus startup, the Generation 4 master reads in the "Microprocessor Not Ready" ID code and generates the "Incorrect initialization of the protocol chip by the microprocessor" error message 0C73 and 0D70 ..0D73	
HE 5.	- The expected ID code can be read in after bus startup.	
HE 6.	Diagnostic signals - The required diagnostic LEDs for this device type (see table) are directly connected to the slave protocol chip and are not controlled via software (with the exception of TR). *)	
HE 7.	- If the protocol chip diagnostic input *I/O Error* ("/StatErr" for IBS SUPI 3) is used, the events that are generated by these diagnostic messages are simulated and the response is checked at the INTERBUS master. ****) The data pattern 0xF0 is output for all OUT data bytes of the test object. This means it is also possible to test module error messages by short-circuiting a digital output.	

HE 1. **L2**	**L2 circuit test** input circuit - Have only approved components been used? *)	
HE 2. **L2**	- **L2** Has the input circuit been implemented exactly as shown in the diagram? 	
HE 3. **L2**	**L2 Circuit test transmitter circuit** - Have only approved components been used? *)	
HE 4. **L2**	- **L2 Has** the transmitter circuit been implemented exactly as shown in the diagram? 	
HE 5. **L2**	**L2 EMC wiring** - Have only approved components been used? *)	

HE 6. **L2**	- **L2 Has** the EMC circuit been implemented exactly as shown in the diagram? 	
HE 7. **L2**	**L2 Additional wiring** for INTERBUS Loop data lines - Have **any other** active and passive components (e.g., Transorb or suppressor diodes, filters, etc.) been implemented on/in the INTERBUS data path in addition to those currently used?	
HE 8. **L2**	**L2 Maximum load** - The device takes the INTERBUS Loop voltage for no more than 1.8 A.	
HE 9. **L2**	- **L2 The** maximum current taken from the INTERBUS Loop supply is stated in the user documentation (user manual).	
HE 10. **L2**	**L2 Direct link** - In this specific area of application the Loop IN to Loop OUT direct link is less than 0.15 Ohm (RL1 + RL2 + 4*contact resistance + conductor paths).	
HE 11. **L2**	- **L2 In** this specific area of application the Loop IN to Loop OUT connection is a continuous current of 5 A.	
HE 12. **L2**	- **L2 INTERBUS** Loop signals are looped back from the input to the output without additional (excluding approved) elements (fuses, resistors, etc.).	
HE 13. **L2**	- **L2 INTERBUS** Loop signals are looped back from the input to the output without additional (excluding approved) elements (fuses, resistors, etc.).	

HE 14. L2	**L2 Functional earth ground connection** - The module electronics only have one functional earth ground to prevent ground loops.	
HE 15. L2	**L2 Potential levels** - An additional voltage for the I/O supply is led to the device, which is also electrically isolated from the Loop supply.	
HE 16. L2	**L2 Protocol chip** - Has an approved type of protocol chip or an approved alternative been used? *)	
HE 17. L2	**HE 1.**	
HE 18. L2	- **L2 Is** a green LED connected **directly** to the DIAG pin?	
HE 19. L2	- **L2 Is** pin 5 of IBS **LPC2** connected via at least one capacitor (3.3µF ... 10µF)?	
HE 20. L2	- **L2 Are** Pin6, Pin7, and Pin8 switched with GND?	
HE 21. L2	**HE 2.**	
HE 22. L2	- **Has an** approved quartz type or an approved alternative *) been used?	
HE 23. L2	- **The quartz** pulse circuit does not supply other components with its clock.	
HE 24. L2	**HE 3.**	
HE 25. L2	- **L2 The** clockline circuit is tested with the same permissible temperature range +/- 10% of the device.	

Manufacturer

Name	Signature

Manufacturer Declaration for Devices With Optical Fiber Interface

Test report number

No.	Test Step	OK *)
HE 1.	24 V supply **voltage loop** from input to output - All 3 signals FE, +24 V, and 0 V must be looped through without any additional elements (fuses, resistors, etc.) from the input to the output.	
HE 2.	- The 24 V supply voltage connection must be designed according to the defined continuous current. - Installation remote bus I_{Nom} = 4.5 A	
HE 3.	- The 24 V supply voltage connection must be designed according to the defined continuous current. - Rugged Line I_{Nom} = 16 A	
HE 4.	Data connection from **the Rugged Line connector** - The length of the shielded cable from the Rugged Line connector to the device electronics should not exceed 20 cm (7.87 in.).	
HE 5.	- Is the shield of the data connection cable for the Rugged Line connector connected to the GND on both sides?	
HE 6.	- The isolation voltage between the individual electrically isolated areas is at least 350 V AC.	
HE 7.	- *) If FE of the outgoing interface is not directly connected with GND, a capacitor/resistor combination (R <= 1 MOhm, C approximately 15nF) (parallel circuit) can be selected as an alternative. **HE** 3.	
HE 8.	- Are all the unused inputs for the protocol chip (including MFPs) connected with a defined voltage?	
HE 9.	- 3Chex - For remote bus devices (for devices with special requirements, only is approved by the INTERBUS Club.)	

HE 10.	- During bus startup, the Generation 4 master reads in the "Microprocessor Not Ready" ID code and generates the "Incorrect initialization of the protocol chip by the microprocessor" error message 0C73 and 0D70 ..0D73	
HE 11.	- The expected ID code can be read in after bus startup.	
HE 12.	- The power-up reset input of the slave protocol chip and the assigned expansion blocks are wired with a 1 kOhm, 100 nF filter.	
HE 13.	- The voltage monitoring circuit ensures that the reset input for the protocol chip and the assigned expansion blocks has a low signal with a voltage of U Nom minus the tolerance (5 V - 10%, typical).	
HE 14.	- The reset time realized by the voltage monitoring circuit is at least 2 oscillator clock cycles (125 ns at 16 MHz, typical) for the balanced oscillator and at specified voltage.	
HE 15.	- For direct and indirect wiring of the reset input, ensure that the components used in the entire voltage area of the voltage monitor are operating properly. Standard logic gates are **not** suitable.	
HE 16.	- The power-up reset of the slave protocol chip and the assigned expansion blocks is never influenced by the software, an LCA or microprocessor.	
HE 17.	- The resistance between +5 V and the reset pin of the IBS SUPI 3 OPC protocol chip family is **never** lower than 600 Ohm.	
HE 18.	- When using the reset pin of the IBS SUPI 3 OPC protocol chip family as an input: The resistance between GND and the reset pin of the protocol chip does not exceed 600 Ohm on a "0" signal.	
HE 19.	- When using the reset pin of the IBS SUPI 3 OPC protocol chip family as an output: The resistance between GND and the reset pin of the protocol chip is not less than 23 kOhm.	
HE 20.	- A clock (e.g., quartz oscillator) applied at the protocol chip meets the requirements given in the INTERBUS protocol chip data sheet. **)	
HE 21.	- A quartz used meets the requirements given in the INTERBUS protocol chip data sheet. ***)	

HE 22.	- A quartz oscillating circuit does not supply other components with its clock.	
HE 23.	- The clockline is not influenced by other logic or software.	
HE 24.	- The clockline circuit is tested for the entire permissible temperature range of the device +/- 10%.	
HE 25.	- Additional capacitors for the IBS SUP13 quartz OPC quartz inputs are not available.	
HE 26.	- Have approved types or an approved alternative been used for the expansion blocks? *)	
HE 27.	- One data output for the register expansion does not drive more than 4 inputs.	
HE 28.	- If a buffer is used for the register expansion signal ClkExR, have identical buffers been used for signal ToExR2?	
HE 29.	- Are the register expansion registers in close proximity to the protocol chip on the same board? The tracks are < 5 cm (1.97 in.).	
HE 30.	- Are the Latch, Data (IN&OUT), Clock, and /ResReg signals for the register expansion blocks only used by the INTERBUS slave protocol chip or by the reset logic that controls it?	
HE 31.	Diagnostic signals - The required diagnostic LEDs for this device type (see table) are directly connected to the slave protocol chip and are not controlled via software (with the exception of TR). *)	
HE 32.	- The green U_L LED is directly controlled by the voltage monitor.	
HE 33.	- If the protocol chip diagnostic input *I/O Error* ("/StatErr" for IBS SUPI 3) is used, the events that are generated by these diagnostic messages are simulated and the response is checked at the INTERBUS master. ****) The data pattern 0xF0 is output for all OUT data bytes of the test object. This means it is also possible to test module error messages by short-circuiting a digital output.	

HE 34.	- If the protocol chip diagnostic input *Reconfiguration Request* ("Conf" for IBS SUPI 3) is used, the events that are generated by this diagnostic message are simulated and the response is checked at the INTERBUS master. ****)	
HE 35.	- If the protocol chip diagnostic input *MAU Warning* ("MAUWS, MAUWR, MAUWH" for IBS SUPI 3) is used, the events that are generated by this diagnostic message are simulated and the response is checked at the INTERBUS master. ****)	
HE 36.	- If the protocol chip diagnostic input *Microprocessor Watchdog* ("/StatErr" for IBS SUPI 3) is used, the events that are generated by this diagnostic message are simulated and the response is checked at the INTERBUS master. ****)	
HE 37.	- If the protocol chip diagnostic output *Alarm* ("Alarm" for IBS SUPI 3) is used, the events that are generated by this diagnostic signal at the device are checked. ****)	
HE 38.	- If the protocol chip diagnostic output *Module Acknowledge* ("/ModAck" for IBS SUPI 3) is used, the events that are generated by this diagnostic signal at the device are checked. ****)	
HE 39.	Additional PCP error **codes** - Additional PCP error codes defined by the manufacturer are always assigned error class "8", error code "0" in the additional code.	

No.	Test Step	OK *)
HE 1 LWL	- All resistors have a tolerance of +/- 1%.	
HE 2. LWL	- All resistors have a tolerance of +/- 10%.	
HE 3. LWL	- All resistors have a tolerance of +/- 1%.	
HE 4. LWL	- All resistors have a tolerance of +/- 1%.	

HE 5. **LWL**	- Have any other active and passive components (e.g., Transsorb or suppressor diodes, filters, etc.) been used on/in the INTERBUS data path in addition to those currently used and specified in the circuit versions?	
HE 6. **LWL**	**Connector pin** assignment - Has an approved connector type been used? *) - Which? (please enter here)	
HE 7. **LWL**	- Has an approved type of protocol chip or an approved alternative been used? *)	
HE 8. **LWL**	- Is optical control enabled? (RF1=RF2=0 for SUPI3 OPC)	

Manufacturer

Name

Signature